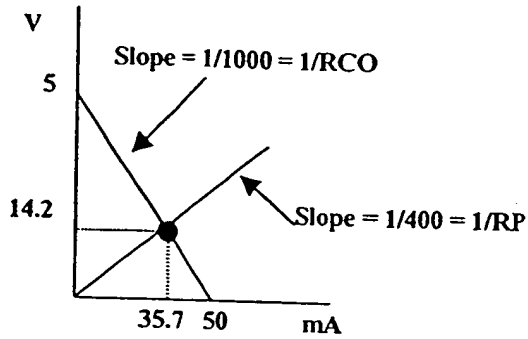


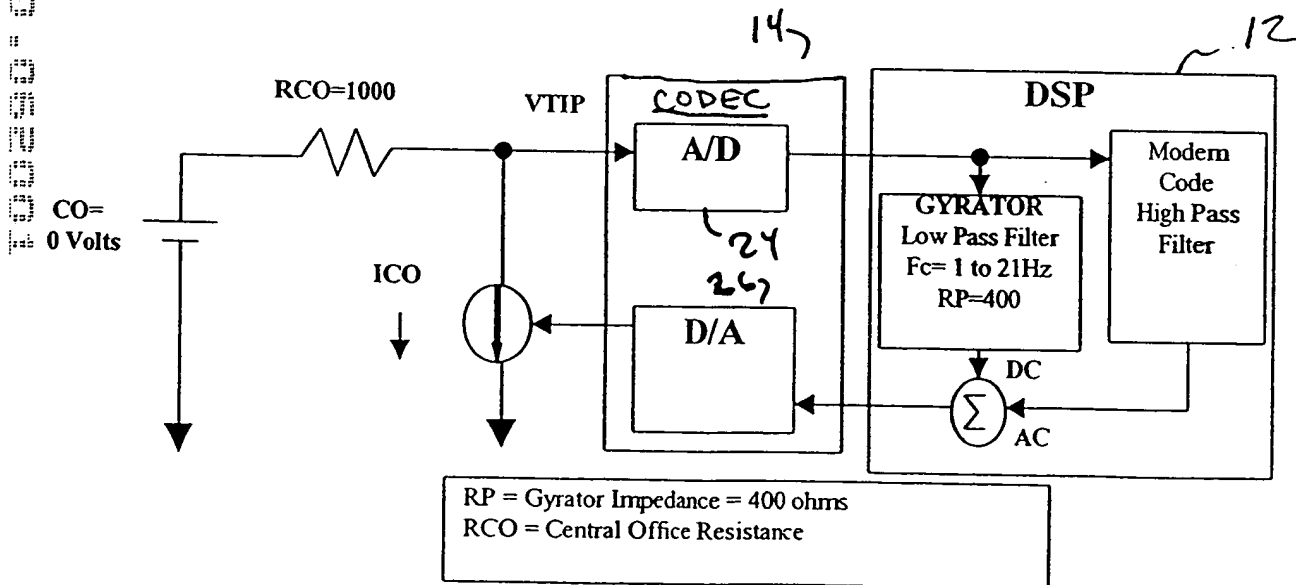
FIG. 1B

V/I Loadline



$50 - ICO \cdot RCO = ICO \cdot RP = VP$
 $ICO = 14.27 \text{ mA}$
 $VP = 35.7 \text{ Volts}$
 Note: All results are at steady state

FIG. 2A



DYNAMICALLY
 ADJUSTABLE
 Digital Gyrator Example

FIG. 2B

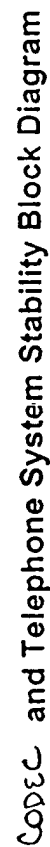
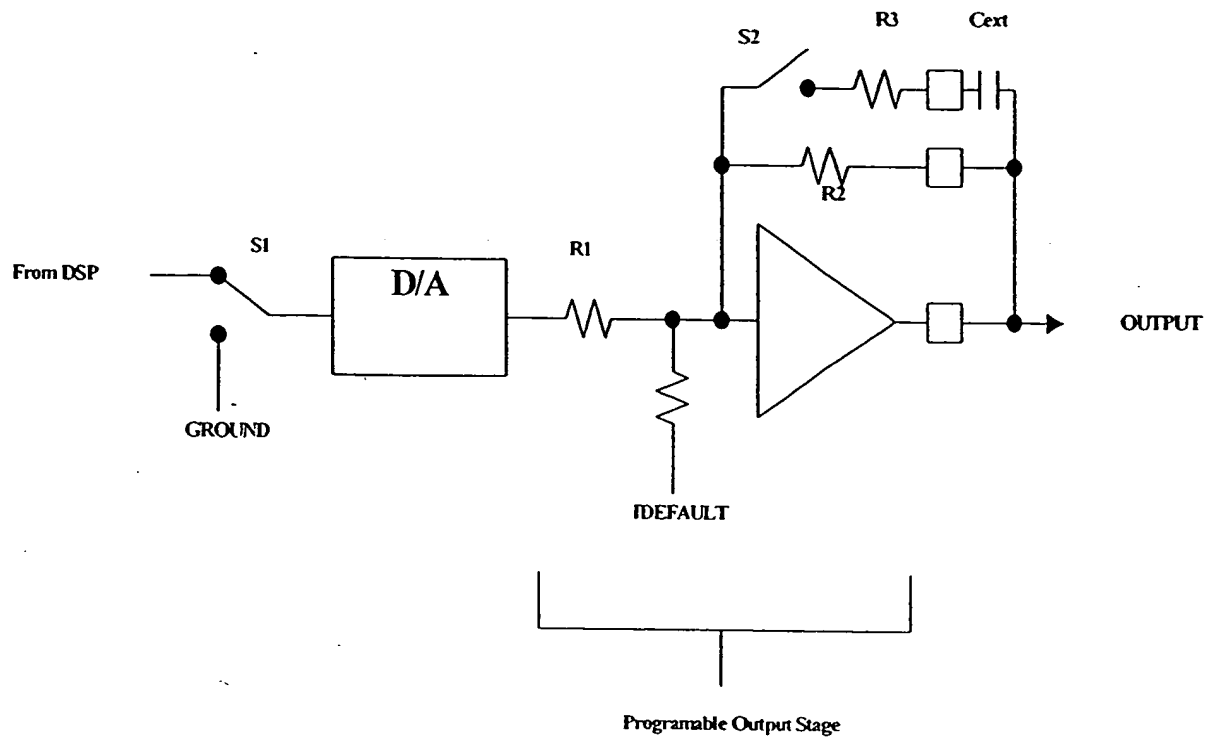


Fig. 3.



Simplified D/A Path

FIG. 4

ADRNG = 1.16
 DCDIV = 130
 DCGN = 5
 DAGN = 1.25
 DARNG = 1.4
 INTGN = .75

Input @ 4.6mV/LSB @TIP

$$1 / (.005 * 32768) = .00611 \text{ mA/LSB}$$

$$H(z) = \frac{\text{Input Gain}}{1 - \text{POLE} * Z^{-1}}$$

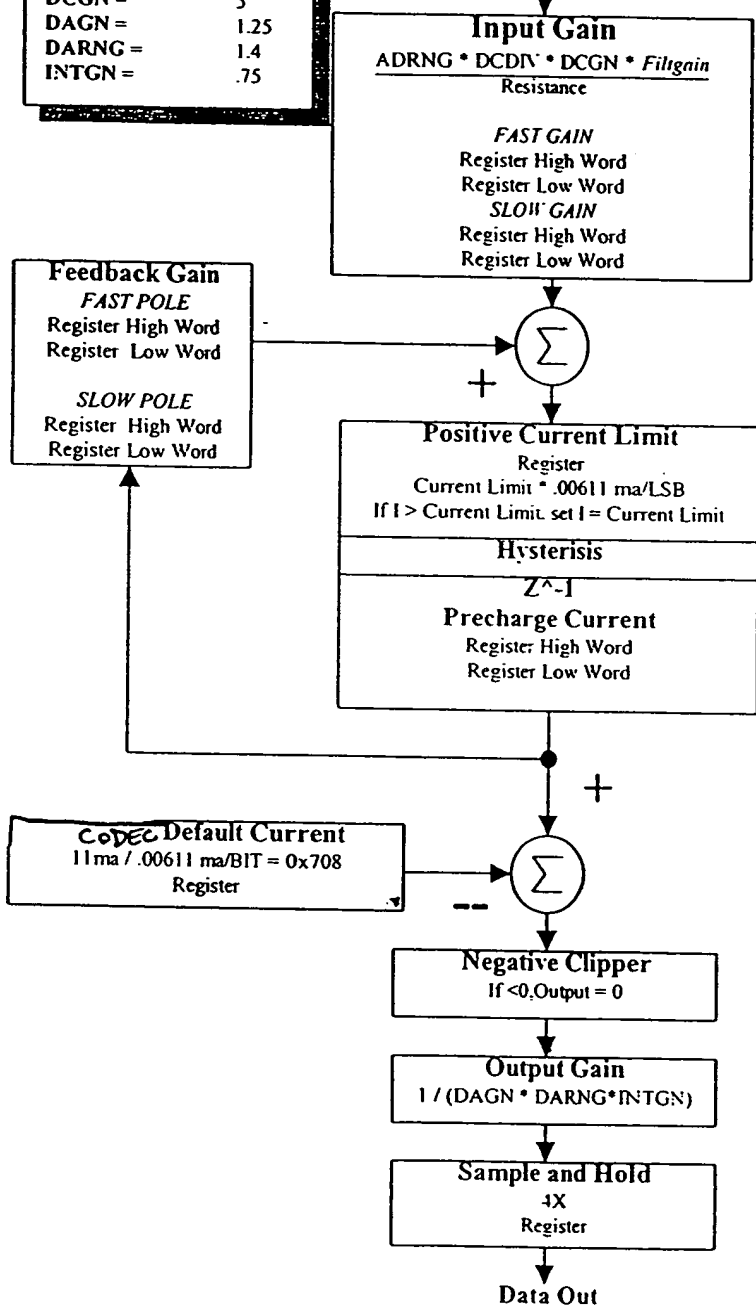


FIG. 6

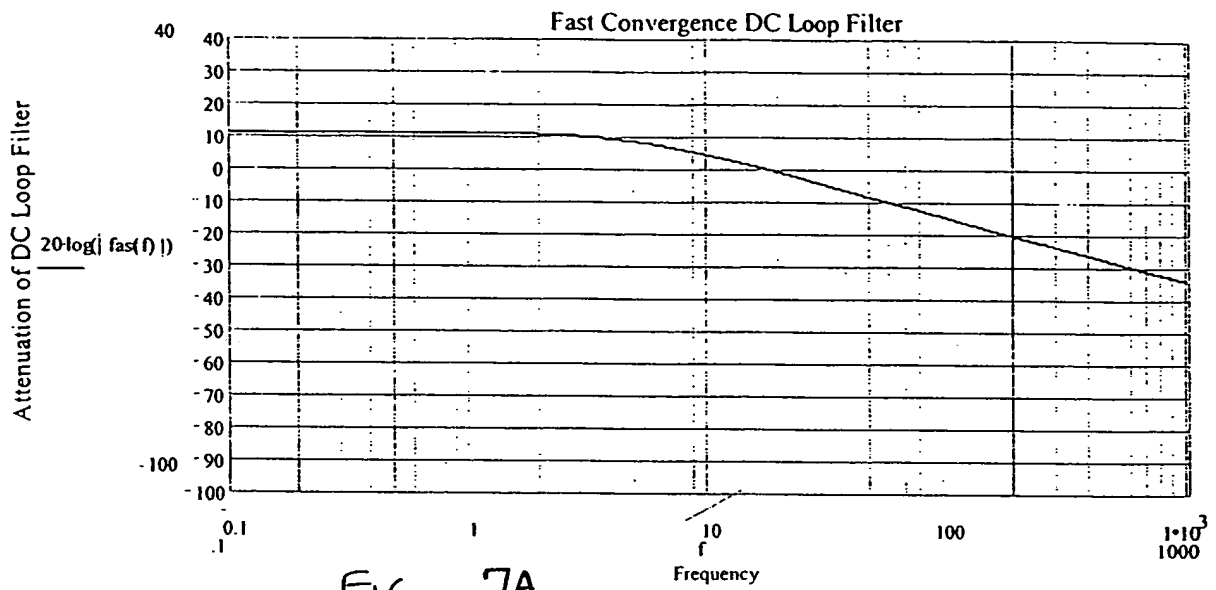


FIG. 7A

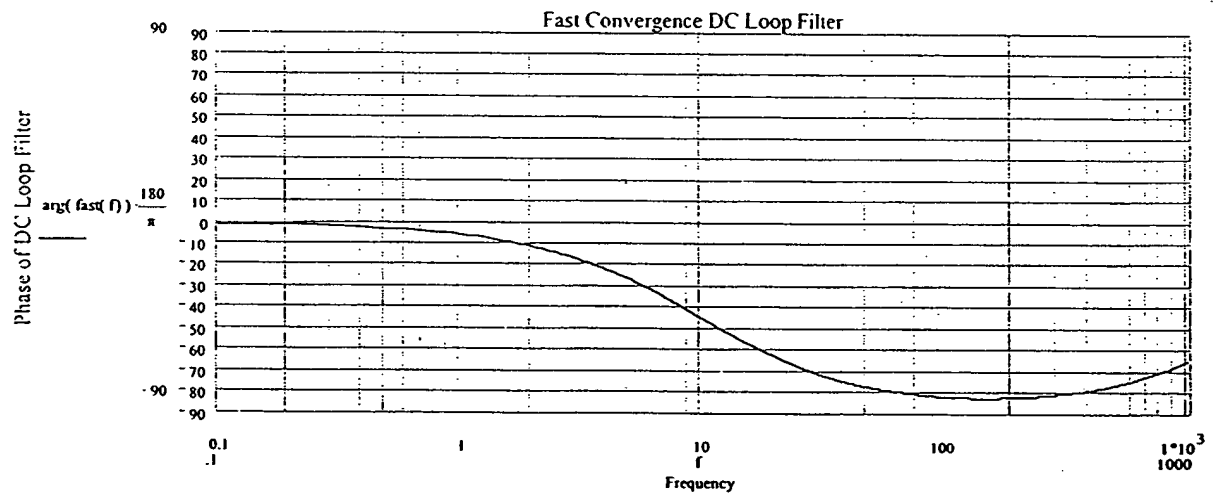


FIG. 7B

10 Hz Fast DC Loop Filter Gain and Phase

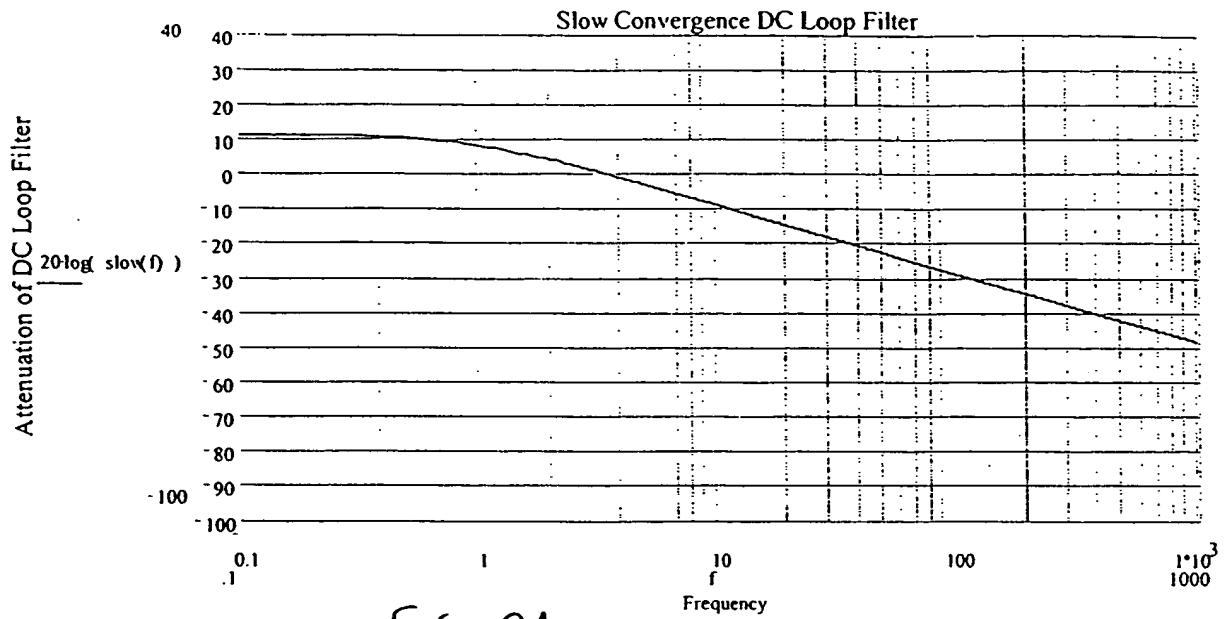


FIG. 8A

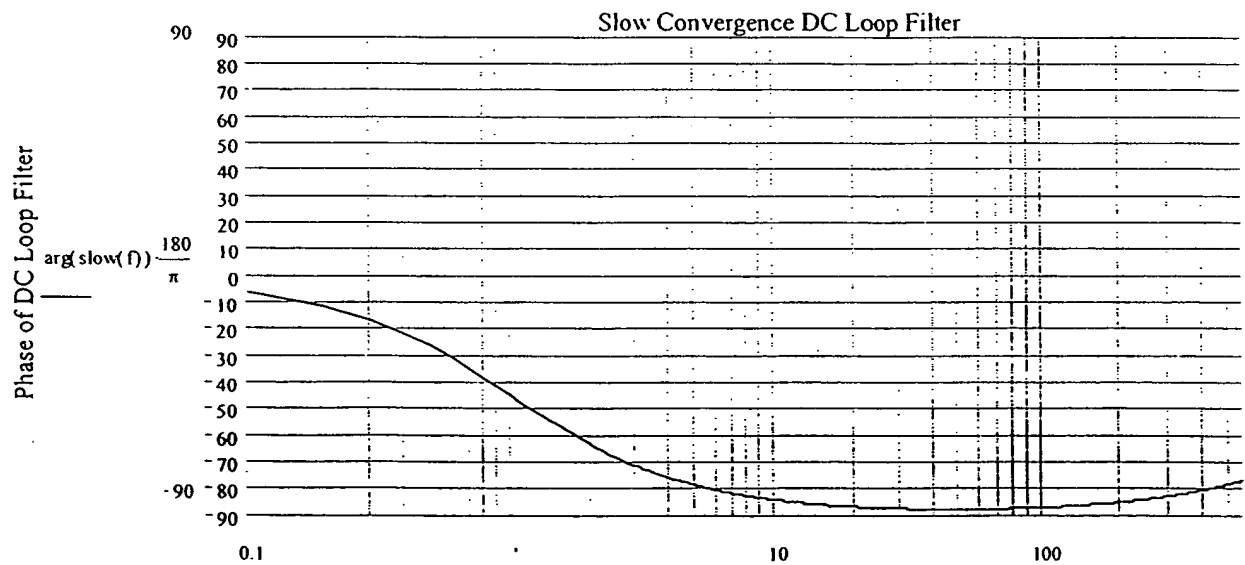
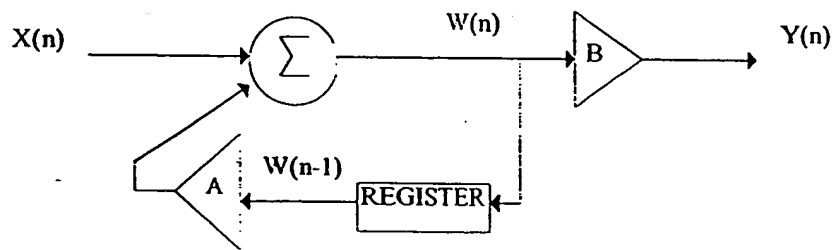


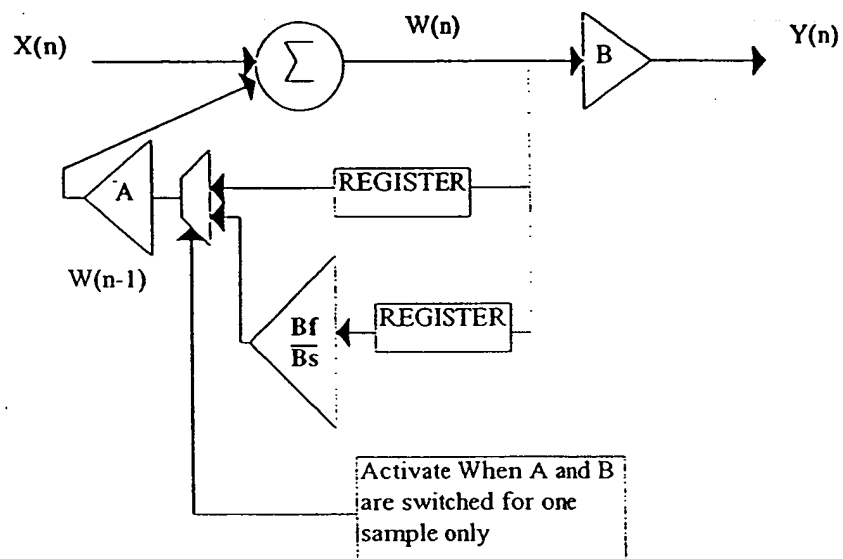
FIG. 8B

1 Hz Slow DC Loop Filter Gain and Phase



First Order Filter Topology

Fig. 9



Final Low Pass Topology with glitch removed

FIG. 10

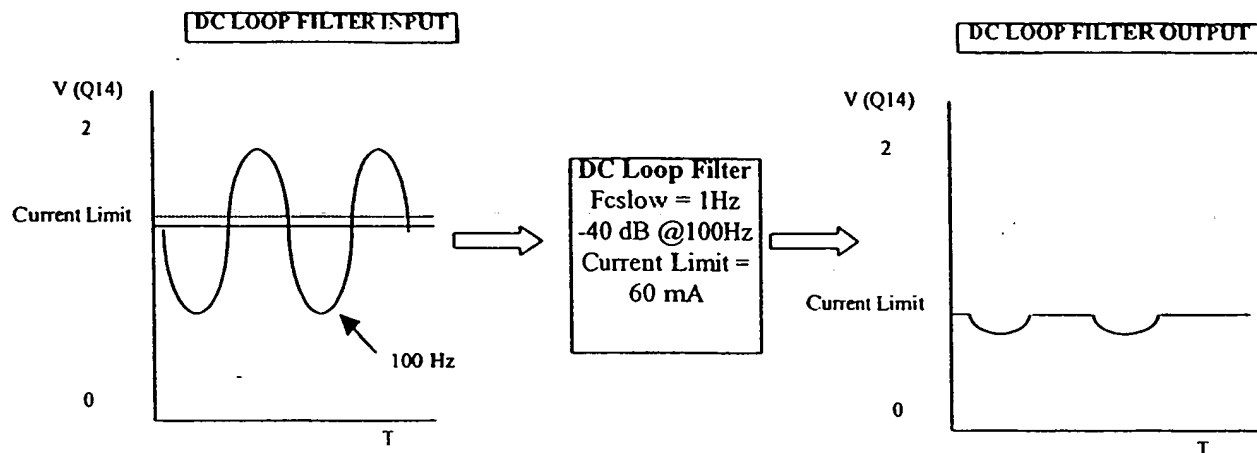


FIG. 11A
 DC Loop Filter Without Hysteresis

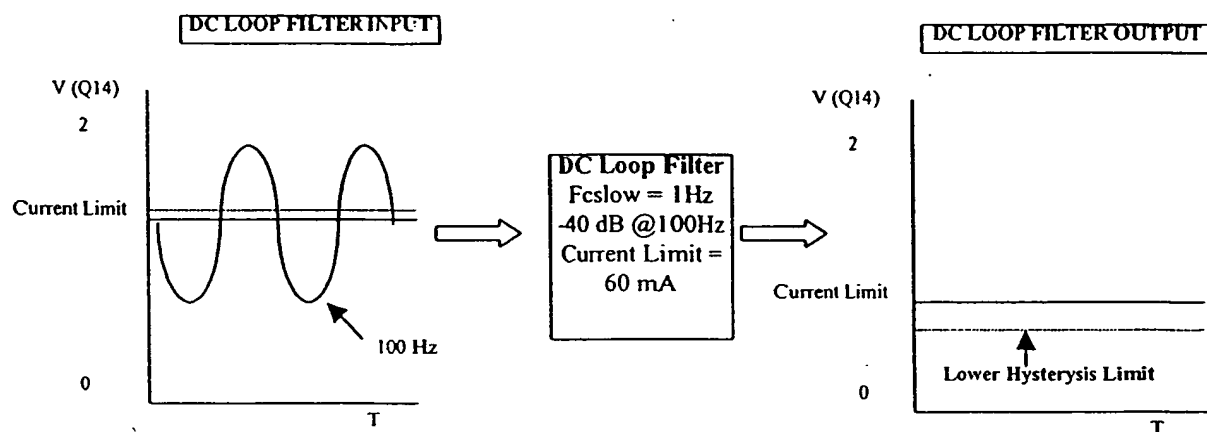


FIG. 11B
 DC Loop Filter With Hysteresis

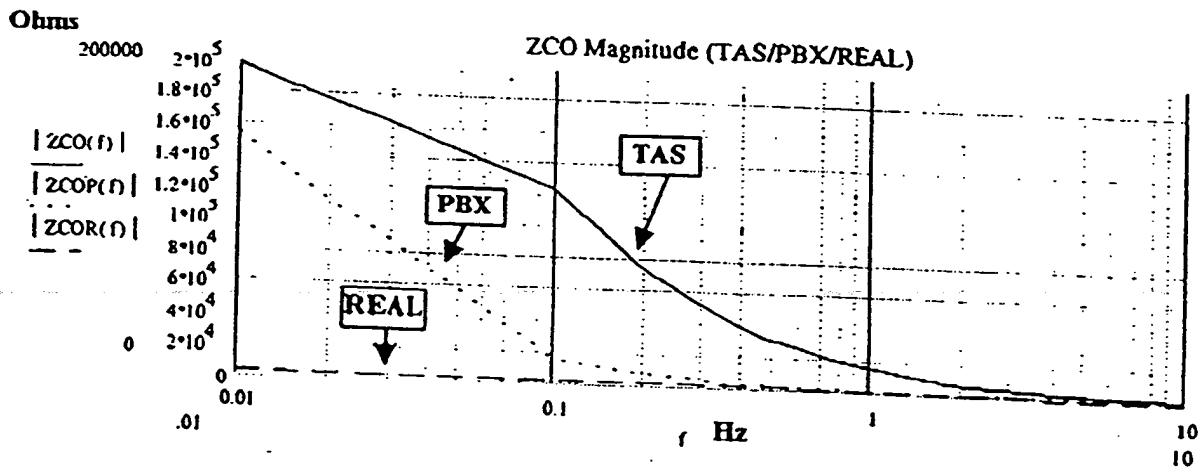


FIG. 12A

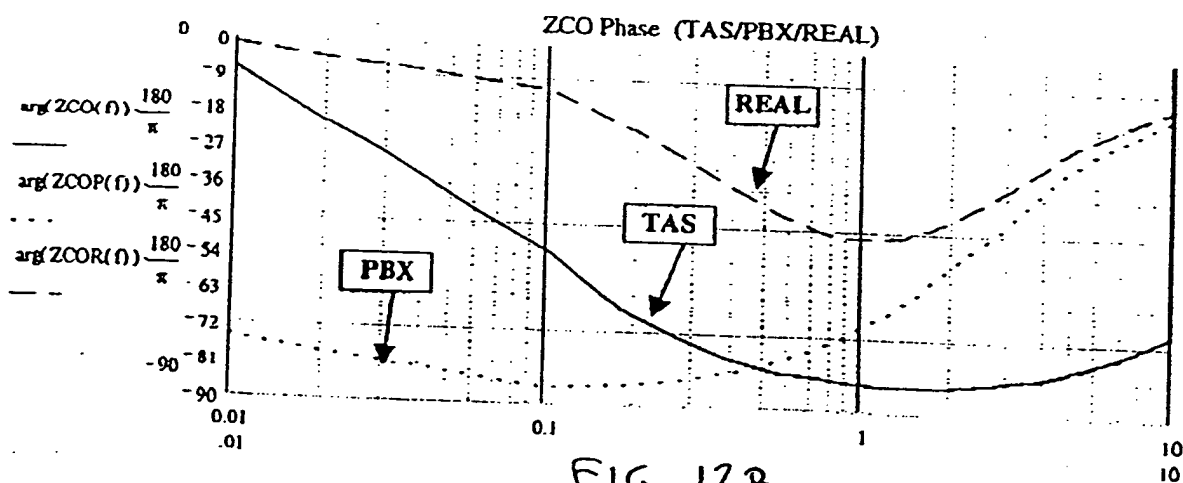


FIG. 12B

TAS, PBX and Real Phone Line V/I Loadlines

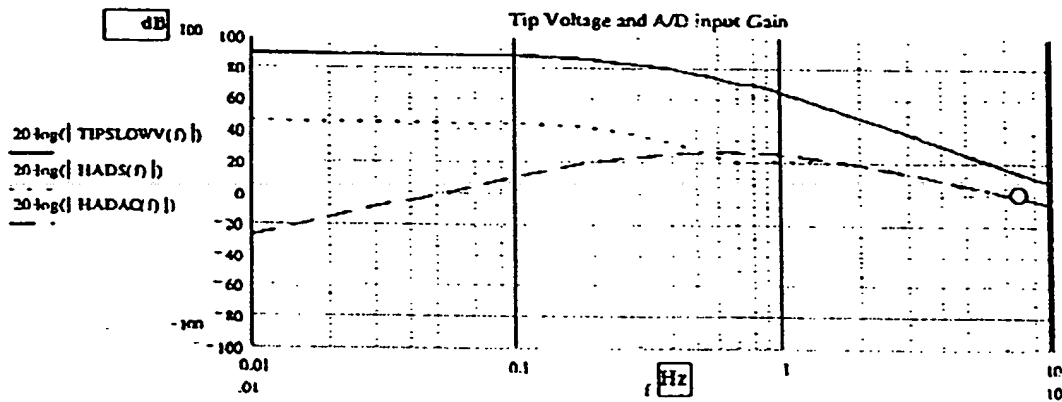


FIG. 13A

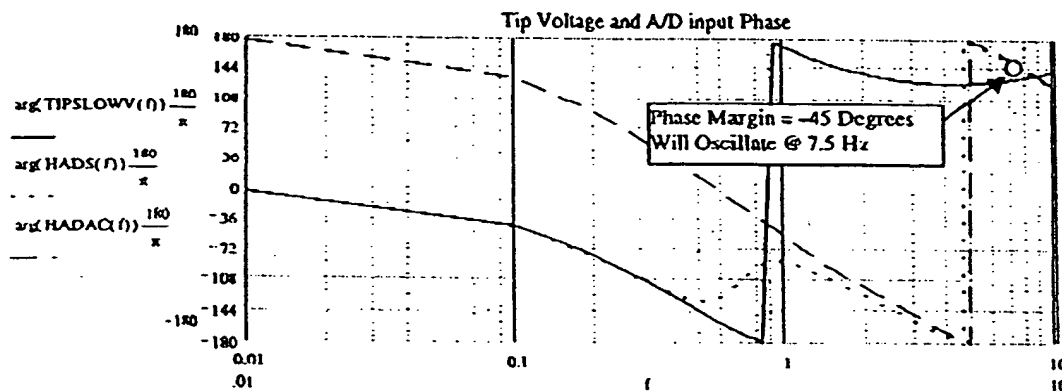


FIG. 13B

TAS Termination with Lowpass Filter Cutoff = 1 Hz

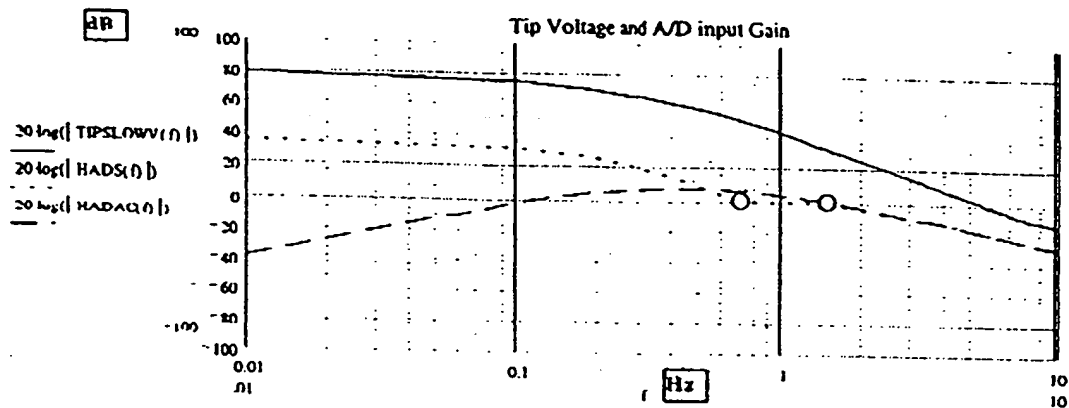


FIG. 14A

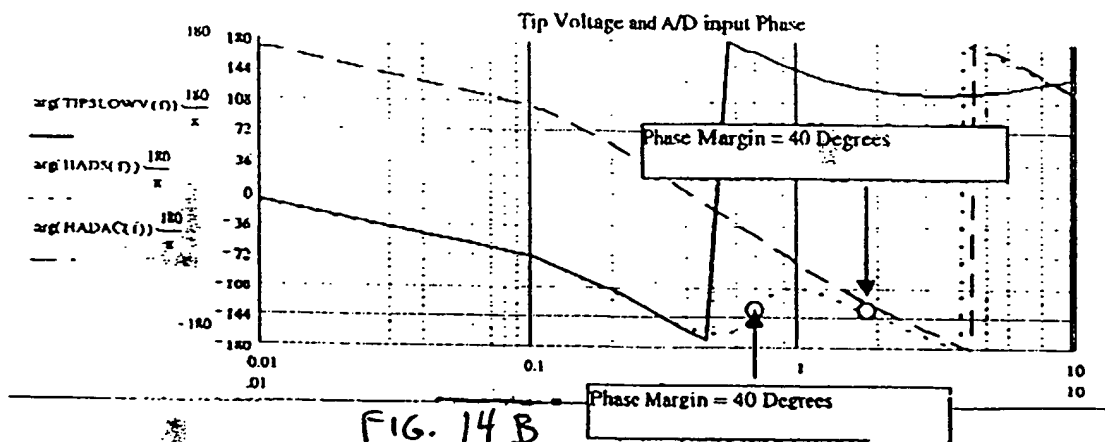


FIG. 14B

TAS Termination with Lowpass Filter Cutoff = .1 Hz

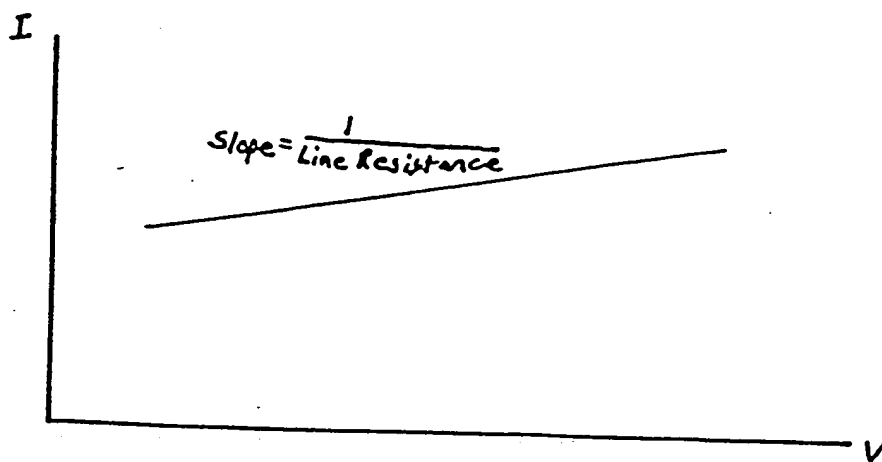


FIG. 15
(PRIOR ART)

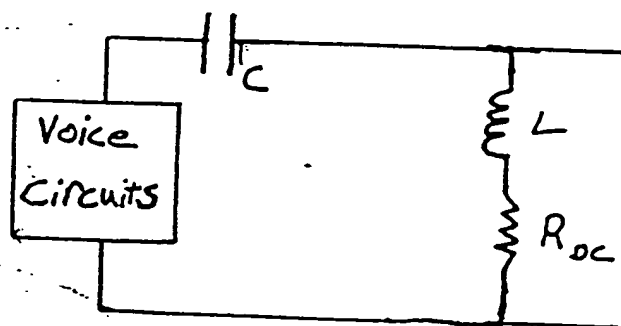


FIG. 16
(PRIOR ART)

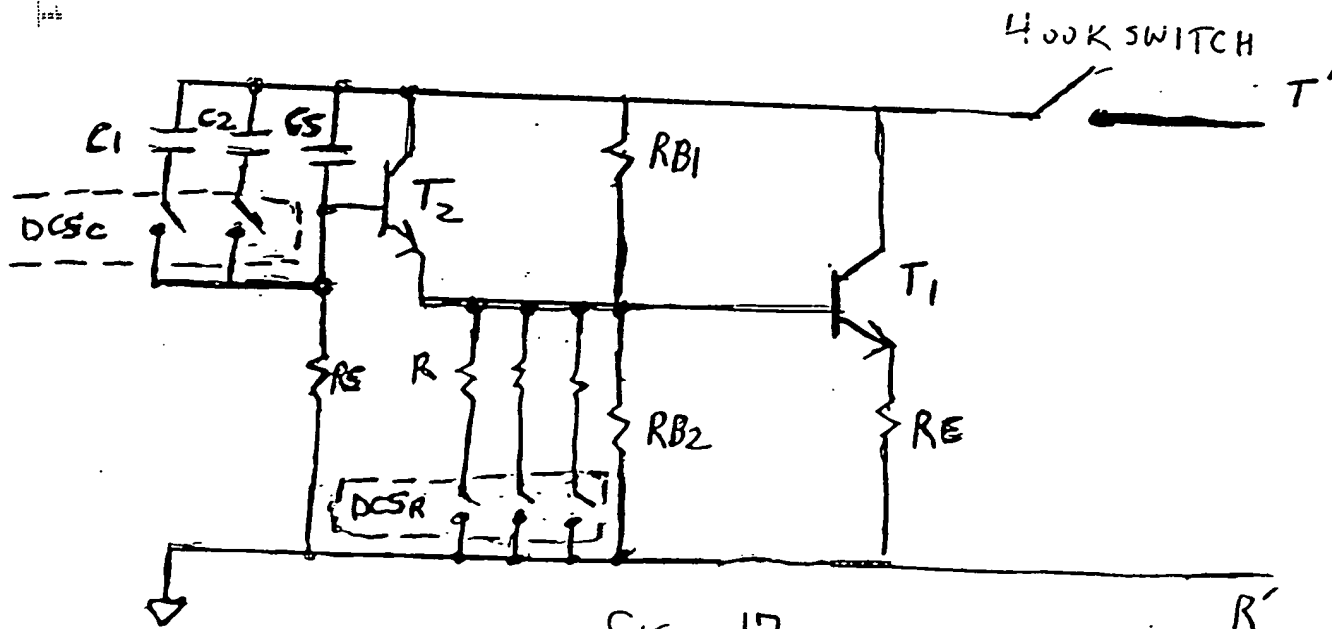
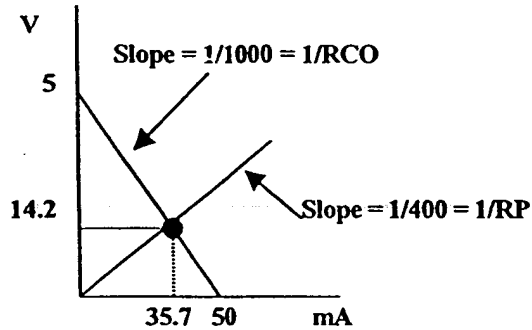


FIG. 17
(PRIOR ART)

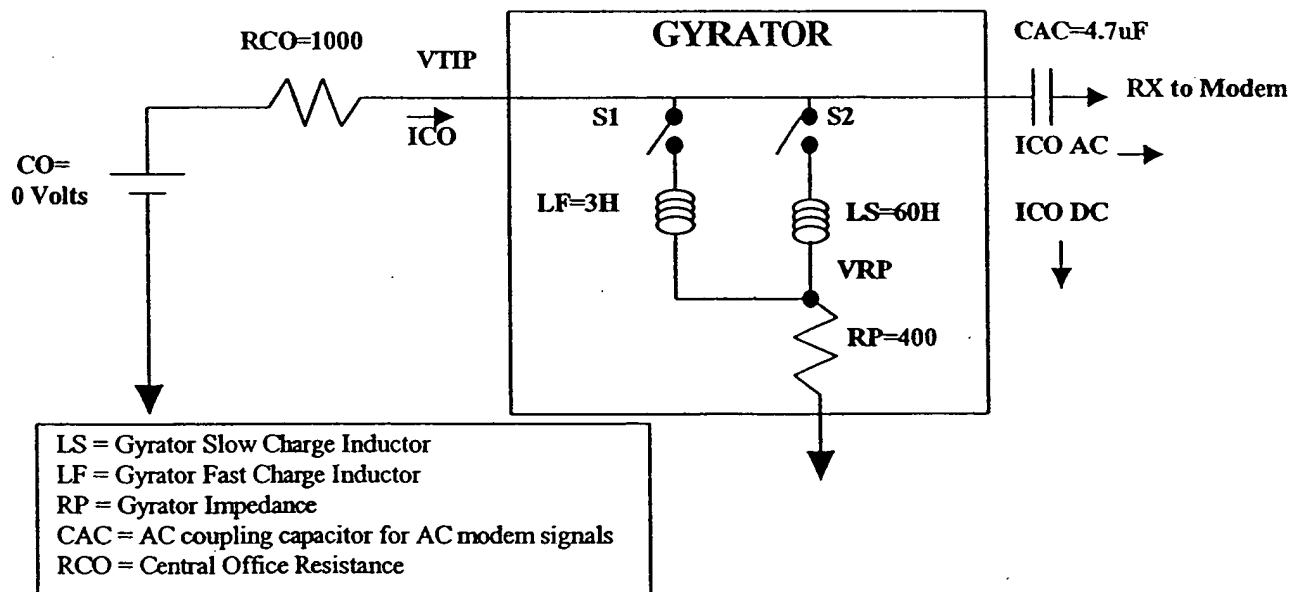
V/I Loadline



$50 - ICO * RCO = ICO * RP = VTIP$
 $ICO = 14.27 \text{ mA}$
 $VP = 35.7 \text{ Volts}$
 Note: All results are at steady state

PRIOR ART

FIG. 18A



Basic External Gyrator Example

FIG. 18B
PRIOR ART